29.8 A Circuit for Reducing Large Transient Current Effects on Processor Power Grids

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At the transistor level, the trend in semiconductor technology has seen the shrinking of device dimensions. This has been accompanied with reduced power supply voltages. At the processor/architecture level, however, the demand for improved processor capability has resulted in increasing transistor counts on the chip. As a result, the power consumption of processor chips has been increasing from generation to generation. This has forced power distribution and management as one of the bottlenecks in the design of current and future processors. One important problem that can arise with increased power consumption is the resultant di/dt effects on the power supply grids. This effect becomes noticeable, for example, when the processor transitions between two frequency modes of operation. The large amount of current consumption change in a short period of time that accompanies such an event can result in a substantial transient voltage swing at the power grid due to parasitic inductances present in the grid as well as in the package. In an environment where the digital power supply can be less than 1V the peak-to-peak transient voltage can become a significant portion of the steady state power supply and critical circuits can fail. Package and circuit designers minimize this effect by adding decoupling capacitors. In this work, we propose a complimentary circuit that can be used to minimize these di/dt effects. This circuit was motivated in part by work presented at ISSCC 2004 [1]. In that approach incremental frequency change is achieved by dithering back and forth between clock sources of different frequencies.

The system level diagram of our circuit is shown in Fig. 29.8.1. It involves a clock source originating from a PLL. This clock source is the input to two dividers: main divider and slow mode divider. The main divider is used in functional mode operation and provides a 50% duty cycle clock to the clock grid. The slow mode divider is designed to provide incremental frequency changes that cover the range between the main divider settings. This allows the user to control the rate at which the clock on the grid transitions between two different frequencies. To eliminate the propagation of runt pulses on the grid during this transition a glitch free multiplexer is used. The presence of the glitch free multiplexer means there will be introduced dead zones on the grid that can last for several cycles while the multiplexer synchronizes the select process. For our application, the dithering approach as described in [1] will result in un-acceptable level of dead zones on the grid due to the synchronization requirements of the glitch free multiplexer. In this work, the glitch free multiplexer makes only two transitions: first when disabling the main divider path and enabling the slow divider path, second when disabling the slow divider path and enabling the main divider path. Hence, for each operating mode change, the dead zone introduced by the glitch free multiplexer is limited to two events.

The slow mode divider introduces incremental frequency change by masking away pulses. Figure 29.8.1 provides a representative example where one clock pulse out of every eight is masked away resulting in an average frequency of 7/8 of the original clock frequency. The slow mode circuit is implemented as a state machine with a fixed set of 8b patterns. Figure 29.8.1 also displays the algorithm the slow mode divider state machine will execute.

A transistor level simulation of the system, shown in Fig. 29.8.1, was carried out using the Powerspice® circuit simulation tool. Behavioral level simulation was carried out using Simulink®. The main divider setting is set to /1 and the clock on the grid is initially at 3GHz. The final target frequency on the clock grid is 300MHz and the final main divider setting is /10. The cycle-to-cycle (C-C) frequency at the node labeled 'Clock Test Point' as well as the power spectral density at 'Clock Grid' in Fig. 29.8.1 is displayed in Fig. 29.8.2. The patterns associated with 3/8, 5/8, 6/8 and 7/8 introduce frequency dithering at 'Clock Test Point'. This is due to the asymmetry of the 1's and 0's present in these patterns. The masking patterns also introduce harmonics on the grid. For a PLL output clock frequency of 3GHz, the lowest fundamental harmonic tones introduced by each masking pattern are: 11101111 (7/8): 375MHz, 11011101 (6/8): 750MHz, 10101101 (5/8): 375MHz, 01010101 (4/8): 1.5GHz, 00100101 (3/8): 375MHz, 00010001 (2/8): 750MHz, and 00000001 (1/8): 375MHz.

Figure 29.8.3 displays a simplified architecture of the slow mode divider circuit. The circuit is implemented using an 8b shift register with parallel data write capability. A state machine is used to control the shift register.

The system shown in Fig. 29.8.1 was implemented in IBM's 90nm partially depleted SOI technology. The die was packaged prior to testing. The maximum clock frequency on the clock grid is 3GHz. The power supply to the chip is provided from a board level voltage regulator with no remote sense feedback to correct for voltage droop. A high impedance voltage sense probe was attached to the chip level VDD to monitor voltage droop during frequency transition. An Agilent 54855A high-speed sampling scope is used to collect the data. Figure 29.8.4 shows the C-C frequency at the test point as well as the measured VDD voltage values. Figure 29.8.5 displays the power spectral density of measured chip level VDD and also that of the measured clock at the 'Clock Test Point'. It also displays the simulated impedance profile of the power distribution network. The frequency axis of the power spectral density of the clock signal at 'Clock Test Point' is multiplied by a factor of 8 to make comparison with the power spectral density of VDD easier. Figure 29.8.6 displays measured transient VDD for a 3GHz to 300MHz frequency transition for a case where slow mode divider circuit is used and for a case where it is not used.

Looking at Fig. 29.8.4 it is apparent the slow mode patters 7/8, 5/8, 3/8 and 1/8 introduce larger VDD noise. These patterns have significant power at 375MHz. This frequency is in the vicinity of the power distribution network resonance. As shown in Fig. 29.8.5, the power distribution network has a relatively broad resonance centered at about 250MHz.

We have demonstrated a circuit that allows for a controlled ramping of frequency with no glitches and minimal amount of dead zones introduced on the clock grid. This reduces large VDD transients by minimizing di/dt rates that can result when a sudden and large frequency change to the clock frequency takes place. Care has to be taken when selecting the masking patterns to avoid stimulating the power distribution network near its resonant frequencies.

References:

[1] Cedric Lichetenau, et al., "Power Tune: Advanced Frequency and Power Scaling on 64B PowerPC Microprocessor," *ISSCC Dig. Tech. Papers*, pp. 356-357, Feb., 2004.

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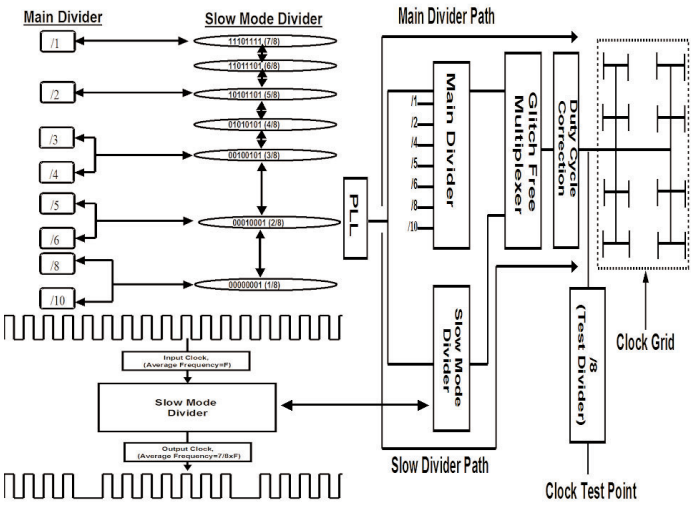

Figure 29.8.1: System level diagram of the clock generation and distribution macro, and also a description of the algorithm executed by the state machine.

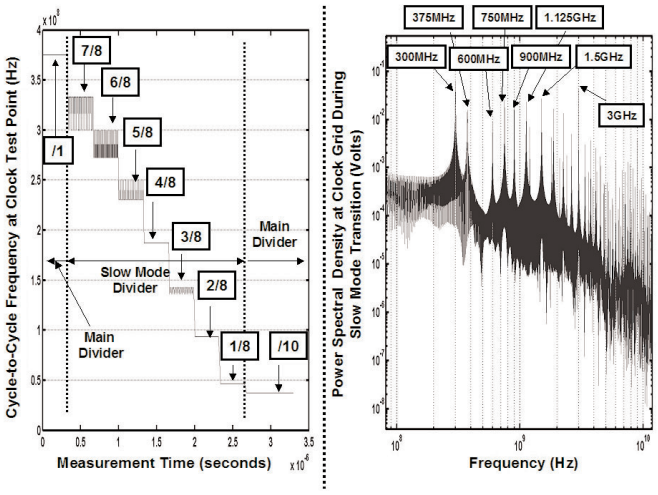

Figure 29.8.2: Cycle-to-cycle frequency at the node labeled 'Clock Test Point' and power spectral density of 'Clock Grid' (from Simulink®).

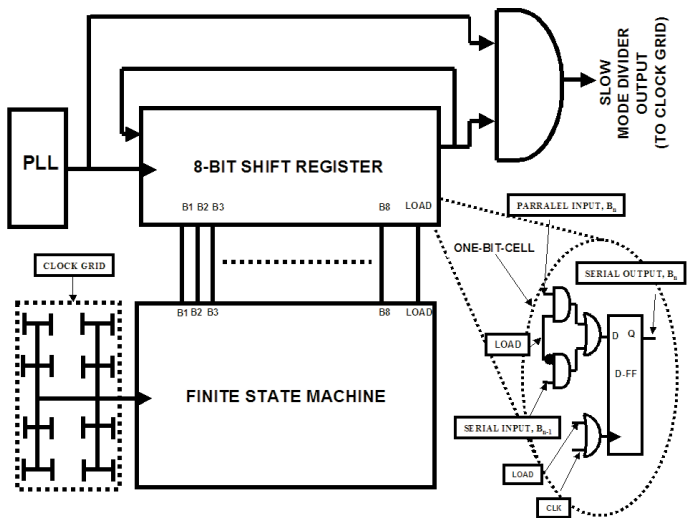

Figure 29.8.3: Simplified architecture of the slow mode divider circuit.

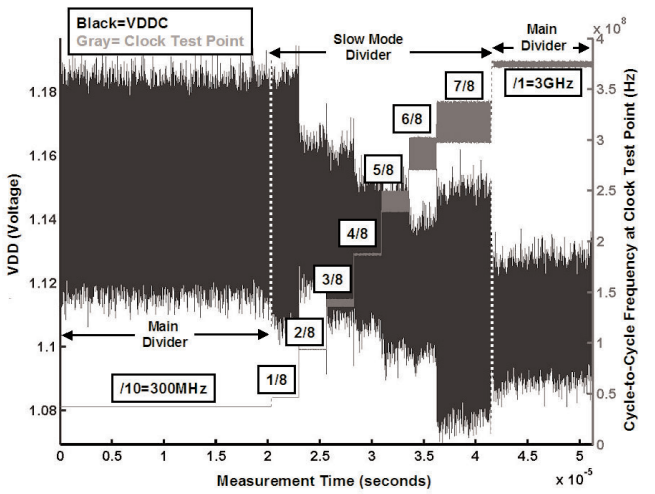

Figure 29.8.4: Measured cycle-to-cycle frequency at 'Clock Test Point' and measured VDD voltage values during a slow mode transition.

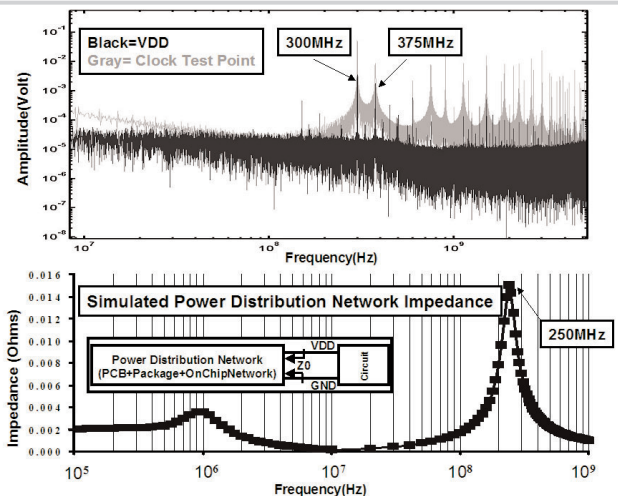

Figure 29.8.5: Measured power spectral density of VDD voltage and also of clock at 'Clock Test Point' during the slow mode transition. To make comparisons easier the frequency axis of 'Clock Test Point' has been multiplied by 8. Bottom: Simulated impedance profile of power distribution network.

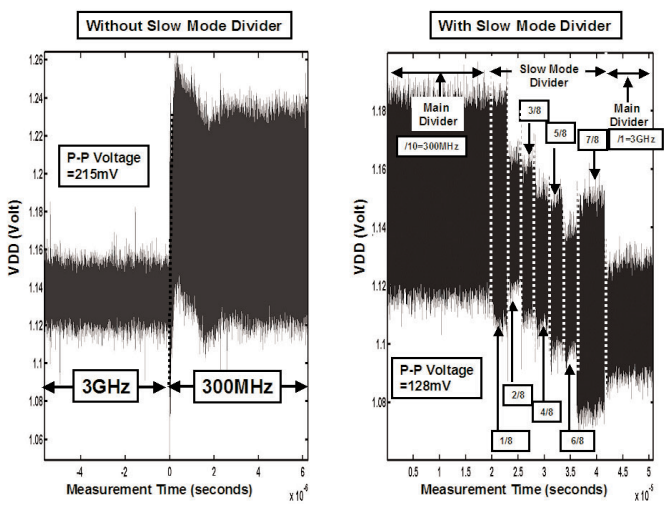

Figure 29.8.6: Measured transient VDD when a direct frequency transition from 3GHz to 300MHz is made (left), and when slow mode divider circuit is used during this transition.